HIBBING COMMUNITY COLLEGE
COURSE OUTLINE

COURSE TITLE & NUMBER: Digital Logic: ENGR 1510
CREDITS: 3 (Lecture 2 / Lab 1)
PREREQUISITES: MATH 2101: Calculus 1

CATALOG DESCRIPTION:
Digital Logic introduces the fundamentals of digital circuits design, including logic gates, Boolean algebra, Karnaugh maps, mathematical operations, flip-flops, and counters. This course is intended for electrical engineering majors and includes laboratory.

OUTLINE OF MAJOR CONTENT AREAS:
1. Number systems and codes
   A. Number systems
   B. Arithmetic
   C. Base conversions
   D. Signed number representation
   E. Computer codes
2. Algebraic methods for the analysis and synthesis of logical circuits
   A. Fundamentals of Boolean algebra
   B. Switching functions
   C. Switching circuits
   D. Analysis of combinational circuits
   E. Synthesis of combinational logic circuits
   F. Computer-aided design of logic circuits
3. Simplification of switching functions
   A. Simplification goals
   B. Characteristics of minimizing methods
   C. Karnaugh maps
   D. Plotting functions in canonical form on the k-map
   E. Simplification of switching functions using k-maps
   F. Product of Sums (POS) form using k-maps
   G. Incompletely specified functions
   H. Using k-maps to eliminate timing hazard
   I. Quine-McCluskey tabular minimization method
   J. Petrick's Algorithm
   K. Computer-aided minimization of switching functions
4. Modular combinational logic
   A. Top-down modular design
   B. Decoders
   C. Encoders
   D. Multiplexers/data selectors
   E. Demultiplexers/data distributors
   F. Binary arithmetic elements
   G. Comparators
   H. Design example: a computer arithmetic logic unit
   I. Computer-aided design of modular systems
   J. Simulation of hierarchical systems

5. Combinational circuit design with Programmable Logic Devices (PLD)
   A. Semicustom logic devices
   B. Logic array circuits
   C. Field-programmable logic arrays
   D. Programmable read-only memory
   E. Programmable array logic
   F. Computer-aided design tools for PLD design

6. Introduction to sequential devices
   A. Models for sequential circuits
   B. Memory devices
   C. Latches
   D. Flip-flops
   E. Other memory devices
   F. Timing circuits
   G. Rapidly prototyping sequential circuits

7. Modular sequential logic
   A. Shift registers
   B. Design examples using registers
   C. Counters
   D. Modulo-N counters
   E. Shift registers as counters
   F. Multiple-sequence counters
   G. Digital fractional rate multipliers

8. Analysis and synthesis of synchronous sequential circuits
   A. Synchronous sequential circuit models
   B. Sequential circuit analysis
   C. Synchronous sequential circuit synthesis
   D. Incompletely specified circuits
   E. Computer-aided design of sequential circuits

9. Simplification of sequential circuits
   A. Redundant states
   B. State reduction in completely specified circuits
   C. State reduction in incompletely specified circuits
   D. Optimal state assigned methods
10. Asynchronous sequential circuits
   A. Types of asynchronous circuits
   B. Analysis of pulse-mode circuits
   C. Analysis of fundamental-mode circuits
   D. Synthesis of fundamental-mode circuits
   E. Introduction to races, cycles, and hazards

11. Sequential circuits with programmable logic devices
   A. Registered programmable logic devices
   B. Programmable gate arrays
   C. Sequential circuit design and PLD device selection
   D. PLD design examples
   E. Computer-aided design of sequential PLDs

12. Logic circuit testing and testable design
   A. Digital logic circuit testing
   B. Fault models
   C. Combinational logic circuit testing
   D. Sequential logic circuit testing
   E. Built-in self-test
   F. Board and system-level boundary scan

COURSE GOALS/OBJECTIVES/OUTCOMES:
1. Students will utilize number systems to perform calculations.
2. Students will explain the fundamentals of Boolean algebra.
3. Students will analyze combinational circuits.
4. Students will plot Karnaugh maps and use the maps in problem analysis.
5. Students will design modular systems.
6. Students will explain flip-flops.
7. Students will analyze sequential logic counters.
8. Students will analyze sequential circuits.
9. Students will perform laboratories to test logic circuits.
10. Students will perform state reduction in specified circuits.
11. Students will analyze asynchronous sequential circuits.
12. Students will perform PLD design.

MNTC GOALS AND COMPETENCIES MET:
N/A

HCC COMPETENCIES MET:
Communicating Clearly and Effectively
Thinking Creatively and Critically

STUDENT CONTRIBUTIONS:
The student will attend class regularly, participate in class discussion, complete assignments, laboratory or design projects, and take a comprehensive final examination. The student will spend sufficient time to complete all assignments.
METHODS FOR EVALUATING STUDENT LEARNING:
The final grade is determined by grades earned on homework problems, laboratory work, periodic examinations, a comprehensive design project, and a comprehensive final examination.

ADDITIONAL INFORMATION:
All homework must be done on engineer's paper.

Curriculum Committee Approval Date: February 12, 2018
AASC APPROVAL DATE: February 21, 2018
REVIEW DATE: February 2023